Study of Common Mode Voltage (CMV) in Three level NPC VSI using SVPWM Techniques

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Abstract— PWM inverters are highly used in motor drive applications in industries. The PWM switching produces common mode voltage (CMV) which in terms produces Common Mode current (CMC). This CMC can cause many adverse effects like EMI and bearing current. The different switching sequences have varying magnitude of common mode voltages. In this paper a comparative study of common mode voltage values of double bus clamping and hybrid bus clamping SVPWM methods are carried out with conventional SVPWM in a Three level VSI. This study further indicates an insight of CMV performance of various switching sequences. The validation of the study is presented using MATLAB simulation and experimental results.

Index terms— Neutral point clamped (NPC), Voltage source inverter (VSI), Space Vector PWM, Common mode voltage (CMV), double bus clamping PWM, hybrid bus clamping method, Switching Sequence.

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1. INTRODUCTION

High frequency pulse width modulation (PWM) techniques are widely used in many ac motor drives to improve the output performance. Most of the ac motor drives work on the earliest PWM techniques which are sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM). The SVPWM technique is considered as a better technique of PWM as it has advantages over SPWM in terms of good utilization of DC bus voltage, reduced switching frequency, low current ripple and better output waveform quality. It is well known that PWM inverters generate high frequency common mode voltage (CMV) with high dv/dt. CMV may cause motor shaft voltages, bearing currents and conduct electromagnetic interference (EMI). The application of two level three phase PWM VSI is limited due to the high dv/dt. The problems of high dv/dt is addressed by using multilevel PWM VSI. The advantages of multilevel VSI as compared to two level are lower voltage stress (dv/dt) on switching device, lower harmonic distortion in output voltage and input current and lower EMI. There are various methods to eliminate CMV using multilevel PWM VSI.

An increased number of voltage level in MLI results in increased switching states. A three level neutral point clamped (NPC) VSI is shown in Fig. 1. The three level NPC VSI has 27 switching states. All the switching states of a three level inverter is shown in Fig. 2. Among these there are seven

switching states that will result in zero CMV. They are six medium vectors (10-1, 01-1, -110, -101, 0-11, 1-10) and one zero vector (000) [1]. However by limiting the switching states only to those switching states to achieve zero CMV, the inverter can not synthesize output voltage as close as possible to sinusoidal waveform. Therefore, the CMV should be reduced to the lowest magnitude level, so that the effect of the same would be less and the drive can work smoothly without any adverse effect. In CSVPWM, the peak value of CMV varies between Vdc/3 to –Vdc/3 with a step size of Vdc/6. For better operation of drive system, the CMV should at least be restricted to Vdc/6 [4]. A modified SVPWM technique is used to reduce the CMV to zero. But these methods use only seven of the 27 vectors that restrict to achieve all the advantages of MLI such as low THD, fewer harmonic in line current etc [2]. Out of 27 voltage vectors only 19 vectors are used which produces CMV value of Vdc/6 or less than that individually and uses only one transition in switching state to limit THD [3]. Voltage vectors those produce CMV zero and Vdc/6 are chosen. However, transition from switching state 1 to -1 introduces more dv/dt and more EMI. Hence to have smooth operation only one switching transition is required [4]. To minimize the CMV, two modulation strategies using one large one medium (OLOM) vectors and zero small medium large (ZSML) vectors have been reported in [5]. One PWM method which eliminates the two zero vectors (111) and (-1-1-1), those produces Vdc/2

and −Vdc/2 as the common mode voltage and uses the other voltage vectors to realize the reference vector [6]. A three dimensional space vector pulse width modulation technique is proposed and various performance parameters are discussed [7]. Three ZCMV methods have been proposed for three phase two level inverter and are compared with the CSVPWM technique [9]. An auxiliary NPC leg implementation method is proposed to reduce the rms value of the CMV with the help of a single phase four winding transformer. But this makes the system bulky and costly [10]. Four single bus clamping methods are proposed and the effect on various performance parameters is discussed [11]. Evaluation of THD using different Hybrid bus clamping methods in three phase two level inverter are discussed in [12]. The study about various switching transitions of SVPWM methods and their effects on CMV form a prior area of interest. This paper focuses on the various switching sequences and their effect on CMV in the output voltage. Section-II of the paper presents a description of three level NPC inverter and mathematical explanation of common mode voltage. Different switching sequences used for study are explained in detail in section-III. In section-IV, simulation results and a comparative study between different SVPWM techniques are presented. Section V concludes the paper.

2. DESCRIPTION OF SVPWM TECHNIQUES AND COMMON MODE VOLTAGE IN A THREE LEVEL VSI

A three-phase three-level Neutral Point-Clamped (NPC) VSI is shown in Fig. 1. A common DC bus is used to feed the three phase. There are two series connected DC link capacitor C1 and C2 are used in the frontend. The DC bus voltage gets divided into three levels using different switching; namely +Vdc/2, 0 and −Vdc/2. The output of all the three phases are these three voltage level produced by appropriate switching of the power semiconductor devices. 'O' is the neutral point of the inverter and also the middle point of the two DC link capacitors. (S1a, S1'a) and (S2a, S2'a) are the two complementary switching devices in the VSI and (D1a, D1'a) are the two clamping diodes per phase. The outer two switches (S1a, S2'a) are responsible for varying pulse width modulation and the inner two switches (S2a, S1'a) are the switches those lamps the output terminal voltage to zero along with the help of the two clamping diodes.

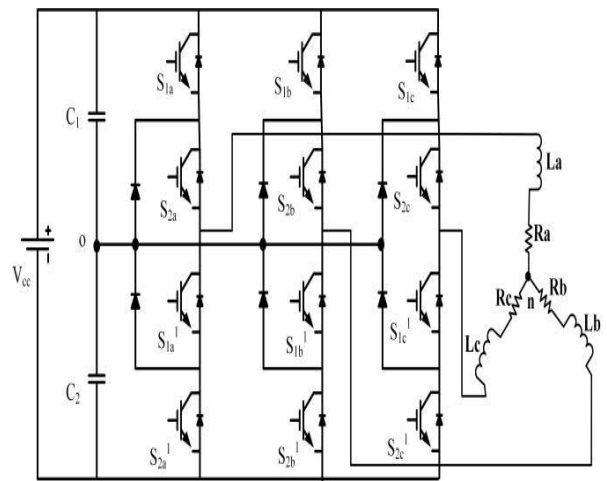Fig.1. Three level NPC VSI

2.1 CONVENTIONAL SVPWM TECHNIQUE

The three level inverter provides three states, those are +Vdc/2, 0 and −Vdc/2. The inverter produces 27 voltage vectors. Unlike two level inverter it doesn't have equal magnitude voltage vector. Hence these are divided into four types based on magnitude. They are named as zero vectors (having a magnitude of 0), 12 small vectors (having magnitude of 0.334Vdc), 6 medium vectors (having a magnitude of 0.577Vdc) and 6 large vectors (having magnitude of 0.667Vdc) respectively. Some vectors have redundant switching state, which means it can be generated using more than one switching state. The space vector diagram of a three level inverter is shown in Fig. 2. The space vector plane is divided into six sectors. Further each sector is divided into four subsectors. When the upper two switches are ON, then the pole voltage is equal to Vdc/2, when the lower two switches are ON, then the pole voltage is equal to −Vdc/2 and when the middle two switches are ON, the pole voltage clamps to 0. The switching states are listed in the Table I.

TABLE.I. Switching states of Three level NPC Inverter

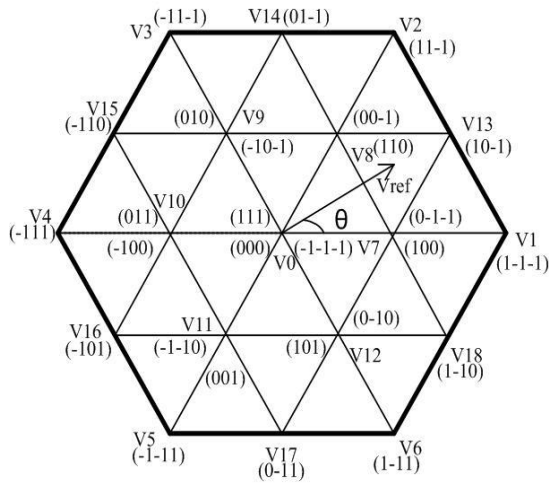| Switching state	S1a	S2a	S1'a	S2'a	Pole voltage
1	ON	ON	OFF	OFF	$V_{dc}/2$
0	OFF	ON	ON	OFF	0
-1	OFF	OFF	ON	ON	$-V_{dc}/2$

Fig.2 Voltage Vector diagram for Three level VSI

TABLE II. CMV for different switching states

Level	Switching states	CMV
+3	111	$V_{dc}/2$
+2	110,101,011	$V_{dc}/3$
+1	1-11,11-1,-111,001,100,010	$V_{dc}/6$
0	000,01-1,-110,1-10,10-1,-101,0-11	0
-1	-1-11,-11-1,1-1-1,00-1,0-10,-100	$-V_{dc}/6$
-2	-10-1,-1-10,0-1-1	$-V_{dc}/3$
-3	-1-1-1	$-V_{dc}/2$

2.2 COMMON MODE VOLTAGE

The Common Mode Voltage (CMV) is defined as the voltage difference between the middle of the DC link capacitor point and the neutral point of the load and is given by the following expression.

$$Vcmv = (Va+Vb+Vc)/3 \qquad (1)$$

Where Va, Vb and Vc are the pole voltage of phase A, B and C respectively.

Both in two level inverter and three level inverter the common mode voltage never adds up to zero and hence it produces high frequency common mode voltage in motor winding. Higher CMV leads to CMC and other unwanted issues, because of which many modulation techniques have been proposed through many years in order to reduce the CMV to appreciate levels [8]. The 27 vectors individually contribute to the common mode voltage. Each of the small vectors, medium vectors, large vectors and zero vectors contribute differently, with different magnitude of common mode voltage. Because the switching of vector happens frequently, this leads to higher CMV in the system. The individual CMV contribution by each of the switching vector varies from each other and is given by

$$V_{cmv} = (Sa+Sb+Sc)*(Vdc/6) \qquad (2)$$

Where Sa, Sb and Sc are the switching state of each leg. The individual contribution of CMV by different voltage vectors are divided into seven categories and are listed in the Table II.

3. STUDY OF SVPWM SWITCHING SEQUENCES

3.1 Double Bus clamping SVPWM technique

As seen in Fig. 2 three zero states (+++, 000 and ---) forms the zero vector. Similarly, the small vectors V7 to V12 can be applied from one of the two corresponding state. Just like in two level VSI each switching sequence starts with a zero vector and ends with a zero vector, in three level VSI for continuous modulation method one small vector is used at starting of switching sequence another small vector is used at the end. Hence, these vectors are called as pivot vectors. A pivot vector is used at all modulation indices. The role of pivot vector in a 3LVSI is similar to that of zero vector in case of a 2LVSI. Here a 3LVSI is controlled as an equivalent 2LVSI, so the redundancy in zero vector V0 is not used. If the reference vector falls within the inner hexagon, the reference vector can be realized using two closest vectors along with the zero vector only, formed by the pivot vectors V7 to V12. So in a three level inverter the zero vector is used only at low modulation indices. But for both low modulation indices and high modulation indices pivot vector can be used. Fig. 3 shows the equivalent two level space vector diagram of the corresponding three level VSI with the pivot vector as center.

In conventional SVPWM scheme, the switching vector starts with a pivot vector and also ends with the same pivot vector. So each sub cycle or half-carrier cycle carries twice the pivot vector. In double bus clamping method the pivot vector is applied only once and one of the other applied vectors twice within a sub cycle. The four sequences are 1012, 2721, 7212, 0121. In all the sequence, only one phase switches for a state transition that reduces the THD to a greater extent.
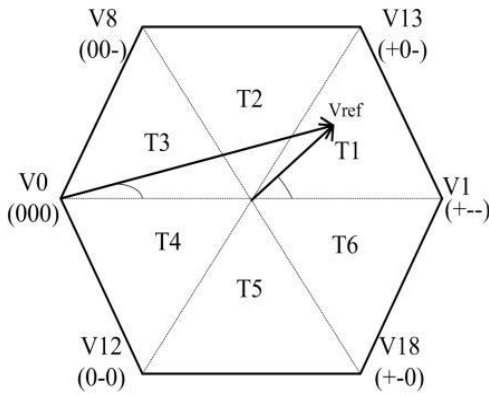
Fig.3. Vector diagram of the equivalent two level inverter in first hextant
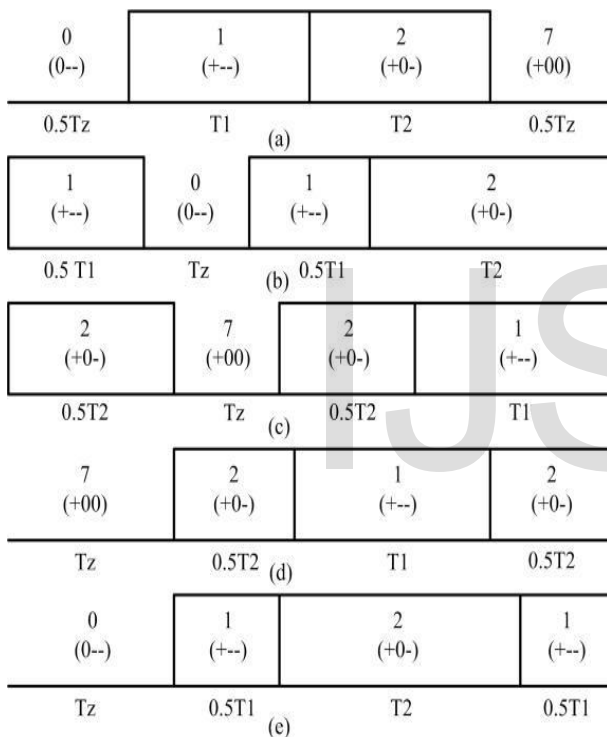

Fig.4. Switching sequence of a three level inverter

Fig. 4 (a) shows the CSVPWM sequence. Fig. 4(b) shows, two times switching happen for R phase where B phase remains switched at one state in the sequence (+--,0-- ,+-- ,+0-).In Fig. 4 (c), the sequence is (+0-,+00,+0-,+--), where R phase remains clamped and B phase switches twice in a sub cycle. In above two cases Y phase switches once. In Fig. 4 (d), the sequence (+00,+0-,+--,+0-), the R phase remains clamped and double switching of Y phase happens. In Fig. 4 (e), B phase remains clamped to the negative DC bus and Y phase is switched twice in one half cycle.

In all the sequences discussed in Fig. 4, for one state transition only one phase is switched. Again, only between adjacent voltage every phase is switched in order to reduce the switching loss and voltage stress low. Table III lists the generalized switching sequence and the corresponding actual switching sequences for triangle T1 to T3 in first hexagon.

TABLE. III. Actual switching sequence in Hexagon 1

Sl. No.	Sequence	Triangle T1	Triangle T2	Triangle T3
1	0127	(0--,+--, +0-,+00)	(0--,00-, +0-,+00)	(0--,00-,000,+00)
2	1012	(+--,0--, +--,+0-)	(00-,0--, 00-,+0-)	(00-,0--, 00-,000)
3	2721	(+0-,+00, +0-,+--)	(+0-,+00, +0-,00-)	(000,+00, 000,00-)
4	7212	(+00,+0-, +--,+0-)	(+00,+0-, 00-,+0-)	(+00,000, 00-,000)
5	0121	(0--,+--, +0-,+--)	(0--,00-, +0-,00-)	(0--,00-,000,00-)

Six bus clamping sequences 20201, 21210, 12120, 10102, 02021 and 01012 are discussed. In all these bus clamping sequences, for some sequences the zero vector and one active vector time are divided equally and for other two active vector time are equally divided in one sub cycle.

3.2 Hybrid Bus clamping method

The above discussed double bus clamping sequences 2721, 7212, 1012, 0121 have been modified and two of them are clubbed together in order to find the hybrid bus clamping sequences. Out of all the sequences, the sequence 0121 or (1210) and 7212 or (2127) are similar that means these sequences apply the zero vector either at the start or at the end of each sub cycle. Similarly, the sequences 1012 or (2101) and 2721 or (1272) are similar, because zero vectors are placed at middle.
When 0121 and 7212 are considered, 0121 sequence gives better result from 0° to 30° in first sector and 7212 gives better result from 30° to 60° based on current ripple analysis. Also for the sequences 1012 and 2721, within 0°

to 30° 1012 gives better result over 2721. Hence, in hybrid sequences first 0121 and 7212 are clubbed with 0121 applied during 0° to 30° and then 1012 and 2721 are clubbed with 1012 applied during 0° to 30° and for the Simulation for all the algorithms is carried out for 8 samples in a half carrier cycle and the modulation index is selected to be 0.8. It is observed that for same number of samples different number of switching happening for each sequence. Details of these algorithms are shown in the Table V. From the table it is clearly seen that the peak value of CMV for 2721 and 7212 are having minimum value of Vdc/6 along with the number of pulses are less. Which implies the number of switching per half carrier cycle is less. Which also indicates the switching losses for these two sequences is minimum as compared to CSVPWM and other sequences.

Next 30° the 2721 sequence is applied [13]. Two other sequences 0121 1012 and 7212 2721 are also considered for study. For all the hybrid sequences, the peak value of common mode voltage (CMV) is studied and the peak value of CMV for all the sequences are compared with the CSVPWM.

4. SIMULATION AND EXPERIMENTAL RESULTS

Simulations are carried out on three level NPC inverter with an induction motor load (4kW 400V 50Hz) using different SVPWM switching sequences in MATLAB/SIMULINK. The SVPWM techniques are implemented with a switching frequency of 1 kHz. The rest of the simulation parameter is shown in the Table IV.

TABLE. IV. Simulation parameters

Parameters	Values
DC link voltage	400V
Switching frequency	1kHz
Fundamental frequency	50Hz
DC link capacitance	2200μF
Modulation index	0.8

The performance evaluation and comparative study is carried out in terms of common mode voltage (CMV) for CSVPWM and the discussed bus clamping methods.

The double bus clamping method with single switching sequence and with combination of two switching sequences is implemented. The result reveals, out of the

four sequences 2721, 7212, 0121, 1012 first two sequence reduces the high frequency common mode voltage significantly as compared with conventional SVPWM. The conventional SVPWM technique causes a high frequency variation of the common mode voltage between different levels, resulting in a high leakage current. These fluctuations are remarkably attenuated using the first two bus clamping sequences. Hence the inverter generates low value of leakage current. However, the latter two sequences generate CMV approximately same as the CSVPWM. So as per the study 2721 and 7212 are minimizing the CMV up to a significant level.

TABLE.V. Performance of NPC inverter for double bus clamping switching sequences

Sequence	No. of Samples	No. of pulse	CMVp(V)
0127	8	14	$V_{dc}/3$
2721	8	11	$V_{dc}/6$
7212	8	12	$V_{dc}/6$
1012	8	14	$V_{dc}/3$
0121	8	13	$V_{dc}/3$
20201	8	24	$V_{dc}/3$
21210	8	14	$V_{dc}/3$
12120	8	16	$V_{dc}/3$
10102	8	19	$V_{dc}/3$
02021	8	25	$V_{dc}/3$
01012	8	18	$V_{dc}/3$

The hybrid bus clamping method implemented is not reducing the common mode voltage up to appreciable value, except 7212 2721, though it gives better result for switching losses and THD. All the hybrid bus clamping methods are implemented with 8 samples in a half carrier cycle. 1012 2721 shows less number of pulses which implies, switching loss is less. Since this method is not suited for CMV reduction, it is not advisable to adopt this

method as far as CMV is concerned. The detail of this algorithm is listed in Table VI.

TABLE.VI. Performance of NPC inverter for hybrid bus clamping switching sequences

sequence	No. of samples	No. of pulses	CMV (V)
1012 2721	8	12	$V_{dc}/3$
0121 1012	8	16	$V_{dc}/3$
7212 2721	8	15	$V_{dc}/6$
0121 7212	8	17	$V_{dc}/3$

A hardware prototype is designed to verify the inverter behavior and the similarity of its output with that of simulation result. The setup consists of the Semikron three level NPC inverter module, driver circuit to drive the IGBT, PIC(PIC18F452) microcontroller for generating the gate pulses, 10 kW 3 phase loading rheostat, DC link capacitors of 2200μf and the D.C supply voltage is approximately 110V. The D.C supply to the inverter module is derived from a three phase bridge rectifier which is connected to the three phase supply. The input is varied through an auto transformer. Design specification of the hardware setup is given in Table VII. Fig. 5 shows the hardware setup of the three level NPC inverter.

TABLE VII. Design specification of hardware setup

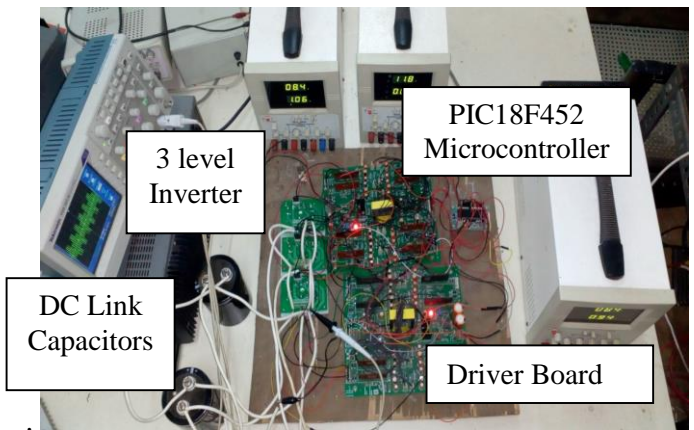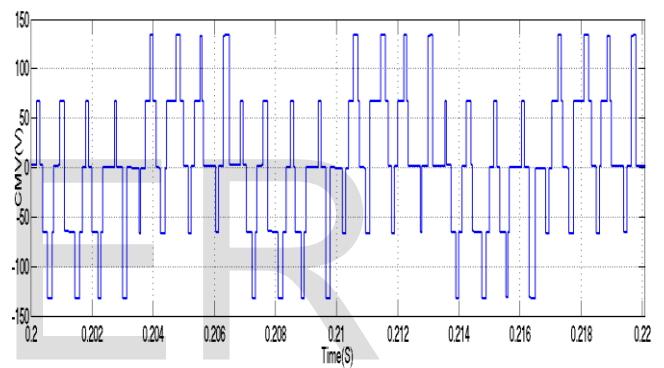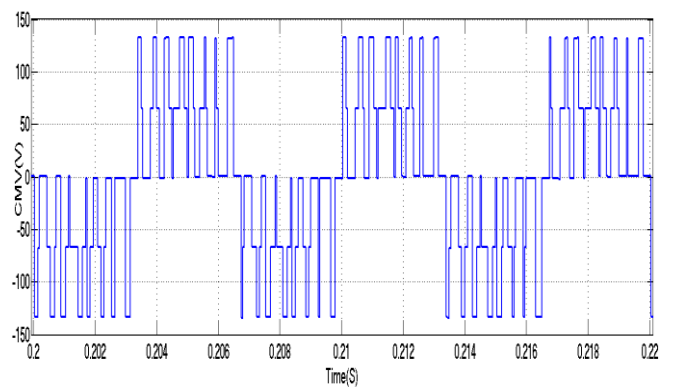| Parameters	Values
Output Power	1kW
Input Voltage	110V
Switching frequency	1kHz
Output frequency	50Hz
DC link Capacitor	2200μf

Fig. 5 Hardware setup for Three level NPC VSI
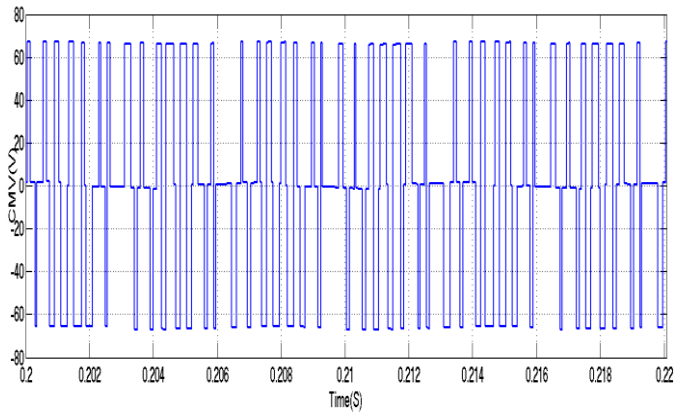
4.1 SIMULATION RESULTS

The simulation and experimental waveforms of CMV for different bus clamping methods are shown below in Fig. 6, Fig. 7 and Fig. 8 respectively.
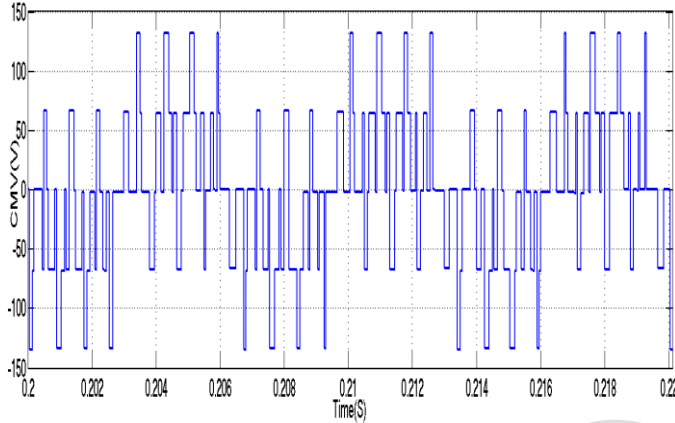

(a)

(b)

(c)

(d)

Fig.6.Waveform of CMV of three level NPC inverter using (a)2721 1012(b)0121 1012(c)7212 2721(d) 0121 7212
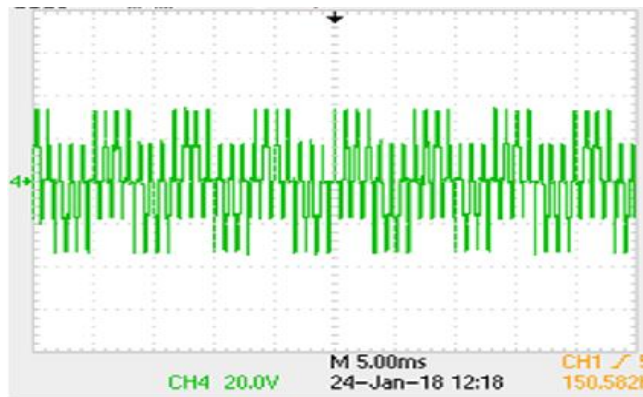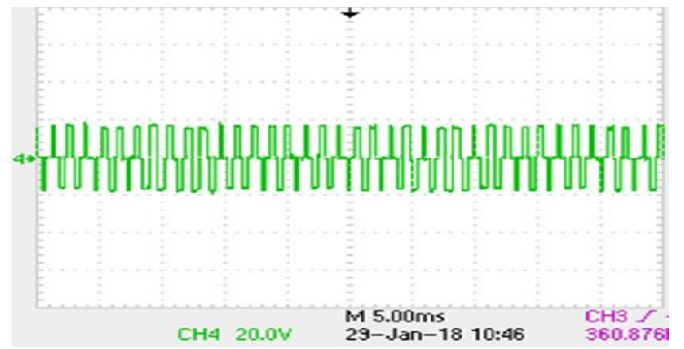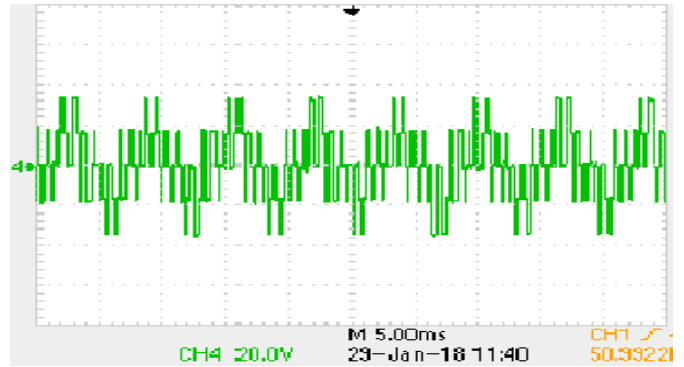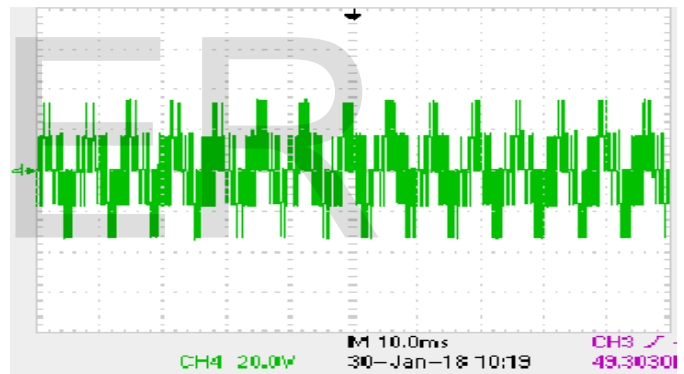
4.2 EXPERIMENTAL RESULTS

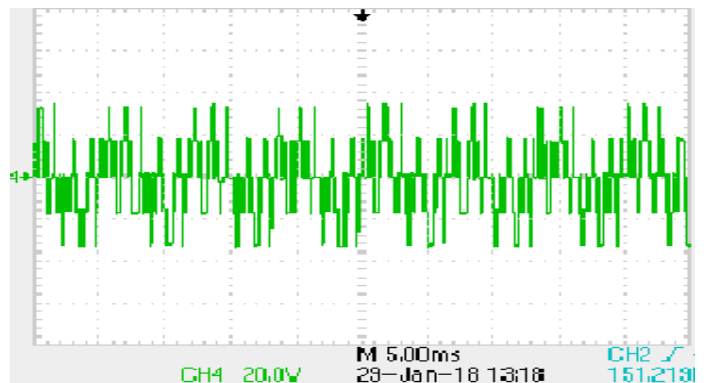Fig.7 Experimental waveform of CMV in CSVPWM

(a)

(b)

(c)

(d)

Fig. 8. Experimental results of CMV for different single bus clamping methods (a) 127 (b) 210 127 (c) 127 210 (d) 210

4.3 COMPARATIVE STUDY

From the above results it can be clearly seen that the peak value of CSVPWM is comparable, since the conventional methods gives the peak value as high as $V_{dc}/3$ with a step size of $V_{dc}/6$. At the same time the above discussed bus clamping method shows for some sequences such as 127 in single bus clamping method, 2721 and 7212 in double bus clamping method, 7212 2721 in hybrid bus clamping method the common mode voltage is getting reduced to the minimum possible level $V_{dc}/6$.

5. CONCLUSION

This paper presents the performance of different SVPWM switching sequences in three level NPC inverter on the basis of the peak value of CMV and also presents a comparative study of the peak value of CMV with the CSVPWM. Out of four double bus clamping sequence 2721,7212,1012,0121 the former two sequences are more effective in terms of CMV and reduce the value up to the possible minimum level Vdc/6. The hybrid bus clamping sequences 7212 2721 is effective to reduce CMV to a value Vdc/6 and other sequences are not reducing the CMV value.

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